the art, the first transistor element **130** and the second transistor element **230** may be transistors of a different type. In such examples, one of the first transistor element **130** and the second transistor element **230** may be covered by a mask which may, for example, comprise a photoresist, while ions are implanted into the other transistor element **130**, **230**.

[0016] After the formation of the active regions **104**, **204**, an oxidation process is performed to form the gate insulation layers **105**, **205**. Thereafter, the gate electrodes **106**, **206** and the cap layers **107**, **207** are formed by deposition, etching and photolithography processes that are well known to persons skilled in the art. Subsequently, the sidewall spacer structures **108**, **208** are formed by depositing a layer of a spacer material and performing an anisotropic etch process wherein portions of the layer of spacer material over substantially horizontal portions of the semiconductor structure **100** are removed, whereas portions of the layer of spacer material provided on the sidewalls of the gate electrodes **106**, **206** remain on the substrate **101** and form the sidewall spacer structures **108**, **208**.

[0017] A schematic cross-sectional view of the semiconductor structure **100** in a later stage of the manufacturing process according to the state of the art is shown in FIG. **1***b*. An etch process is performed. The etch process can be an isotropic etch process adapted to selectively remove the material of the substrate **101**, leaving the material of the cap layers **107**, **207** and the sidewall spacer structures **108**, **208** substantially intact, for example, a known dry etch process. The cap layer **107** and the sidewall spacer structures **108**, **208** protect the gate electrodes **106**, **206**, the gate insulation layers **105**, **205** and channel regions of the transistor elements **130**, **230** below the gate electrodes **106**, **206** from being affected by an etchant used in the etch process.

[0018] Portions of the substrate **101** adjacent the gate electrodes **106**, **206**, however, are etched away. Thus, a source side cavity **110** and a drain side cavity **111** are formed adjacent the gate electrode **106** of the first transistor element **130**. Similarly, adjacent the gate electrode **206** of the second transistor element **230**, a source side cavity **210** and a drain side cavity **211** are formed. Due to the isotropy of the etch process, portions of the substrate **101** below the sidewall spacer structures **108**, **208** and, optionally, also portions of the substrate **101** below the gate electrodes **106**, **206** are removed. Therefore, the cavities **110**, **111** may extend below the sidewall spacer structures **108**, **208** and/or the gate electrodes **106**, **206**.

[0019] Subsequently, stress-creating elements **114**, **115** are formed adjacent the gate electrode **106** of the first transistor element **130**, and stress-creating elements **214**, **215** may be formed adjacent the gate electrode **206** of the second transistor element **230**. To this end, the cavities **110**, **111**, **210**, **211** are filled with a layer of a stress-creating material. In methods of forming a field effect transistor according to the state of the art, the stress-creating material may comprise silicon germanide. As persons skilled in the art know, silicon germanide is an alloy of silicon (Si) and germanium (Ge). Other materials may be employed as well.

[0020] Silicon germanide is a semiconductor material having a greater lattice constant than silicon. When silicon germanide is deposited in the cavities **110**, **111**, **210**, **211**, however, the silicon and germanium atoms in the stress-creating elements **114**, **115**, **214**, **215** tend to adapt to the lattice constant of the silicon in the substrate **101**. Therefore, the lattice constant of the silicon germanide in the stress-creating elements **114**, **115**, **214**, **215** is smaller than the lattice constant of a bulk silicon germanide crystal. Thus, the material of the stress-creating elements **114**, **115**, **214**, **215** is compressively stressed.

[0021] The stress-creating elements **114**, **115**, **214**, **215** may be formed by means of selective epitaxial growth. As persons skilled in the art know, selective epitaxial growth is a variant of plasma enhanced chemical vapor deposition wherein parameters of the deposition process are adapted such that material is deposited only on the surface of the substrate **101** in the cavities **110**, **111**, whereas substantially no material deposition occurs on the surface of the sidewall spacer structures **108**, **208** and the cap layers **107**, **207**.

[0022] Since the stress-creating elements **114**, **115**, **214**, **215** are compressively stressed, they exhibit a force to portions of the substrate **101** in the vicinity of the gate electrodes **106**, **206**, in particular to portions of the substrate **101** below the gate electrodes **106**, **206** wherein channel regions of the transistor elements **130**, **230** are to be formed. Therefore, a compressive stress is created below the gate electrodes **130**, **230**.

[0023] FIG. **1***c* shows a schematic cross-sectional view of the semiconductor structure **100** in yet another stage of the manufacturing process according to the state of the art. After the formation of the stress-creating elements **114**, **115**, **214**, **215**, the sidewall spacer structures **108**, **208** are removed. Additionally, the cap layers **107**, **207** may be removed. Thereafter, an extended source region **116** and an extended drain region **117** are formed in portions of the substrate **101** and the stress-creating elements **114**, **115** adjacent the gate electrode **106** of the first transistor element **130** by means of an ion implantation process known to persons skilled in the art. Additionally, in the ion implantation process, an extended source region **216** and an extended drain region **217** may be formed adjacent the gate electrode **206** of the second transistor element **230**. In the ion implantation process, ions of a dopant material are introduced into the substrate **101** and the stress-creating elements **114**, **115**, **214**, **215**. In case of the formation of N-type field effect transistors, ions of an N-type dopant are introduced, whereas ions of a P-type dopant are provided in the formation of P-type transistors. If the first transistor element **130** and the second transistor element **230** are transistors of a different type, two sequential ion implantation processes may be performed to introduce dopant ions of different type into the first transistor element **130** and the second transistor element **230**. In each of the ion implantation processes, one of the first transistor element **130** and the second transistor element **230** may be covered by a mask absorbing ions and thus protecting the respective transistor element **130**, **230** from being irradiated with ions. The mask may, for example, comprise a photoresist.

[0024] Subsequently, second sidewall spacer structures **108**, **208** may be formed adjacent the gate electrodes **106**. Thereafter, one or more further ion implantation processes may be performed to form source regions **120**, **220** and drain regions **121**, **221** in the first transistor element **130** and the second transistor element **230** by introducing dopant material ions.

[0025] Thereafter, an annealing process may be performed to activate the dopant materials introduced in the formation of the extended source regions **116**, **216**, the extended drain regions **117**, **217**, the source regions **120**, **220** and the drain regions **121**, **221**.